Update on CHIPS Research and Development



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CHIPS R&D Vision



U.S. Technology Leadership

The U.S. invents, develops, and deploys the foundational semiconductor technology of the future.



Accelerate Ideas to Market

A thriving ecosystem that is focused on getting the best ideas to commercial scale as quickly and cost effectively as possible.



A new generation of skilled workers, inventors, designers, researchers, technicians, and others able to build and sustain semiconductor manufacturing in the U.S.



Research & Development

- Strengthen and advance
 U.S. leadership in R&D
- An integrated ecosystem
 that drives innovation
- In partnership with industry, academia, government, and allies
- A strategic view of R&D infrastructure, participant value-proposition, and technology focus areas
- Informed by the Industrial Advisory Committee



Program Development Approach

- Build a national-scale innovation ecosystem
- Build and connect programs in stages
- Invest in the interfaces
- Invest in people







National Semiconductor Technology Center



Vision: Will serve as the **focal point** for research and engineering throughout the semiconductor ecosystem, advancing and enabling disruptive innovation to provide U.S. leadership in the industries of the future.



Structure: A public-private consortium as an independent entity with a governing board informed and advised by industry, academia, government, and key stakeholders.

environment, challenges related to scaling, start-up company support, or

development of advanced manufacturing tools and processes.

- Focus research and engineering on challenging projects with a time horizon beyond 5 years.
- The NSTC will serve as a key convening body for the ecosystem. •

Process:

- NSTC white paper, 1st quarter 2023.
- Summarize the results of a landscape analysis, outline a governance structure, and describe a preliminary operating and financial model.

National Semiconductor Technology Center

Elements:

Core of centrally operated, in-house research, engineering, and program capabilities combined with a network of directly funded and affiliated entities.









National Advanced Packaging Manufacturing Program



- Strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem
- Leverage public-private partnerships, that can include support for facilities managed by the NSTC and MUSA
- Broad range of technologies:
 - Heterogeneous integration
 - Wafer and panel-based approaches
 - Tooling and automation
 - Substrate technology

NAPMP Target Areas



Technology innovation

Create an R&D environment advancing the state-of-the art in advanced packaging.

Ecosystem support

Investments to bolster the growth in domestic capacity and enhance capabilities for competitive edge.



Manufacturing USA Institute(s)





- Up to three new public-private partnership institutes in the Manufacturing USA network
- To advance research and commercialization of semiconductor manufacturing technologies
- Pre-competitive collaboration among researchers and manufacturers
- Ex: Virtualization, simulation, and automation; packaging
- Workforce training

Manufacturing USA Institute Network

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RFI for Manufacturing USA Semiconductor Institutes



Purpose: inform design of up to three Manufacturing USA semiconductor institutes authorized by CHIPS Act

Three public webinars held with 463 registered participants

93 comments received*

Public comment period Oct. 13 – Dec. 12, 2022

Public report to be submitted for clearance early March



*all comments received are publicly posted at <u>https://www.regulations.gov/docket/NIST-2022-0002/comments</u>

NIST Metrology R&D







Strategic Opportunities for U.S. Semiconductor Manufacturing

Facilitating U.S. Leadership and Competitiveness through Advancements in Measurements and Standards

August 2022



- Measurement science for new materials and packaging
- Physical metrology for next-generation microelectronics
- Computation and data
- Virtualization and automation
- Reference materials and data, and calibrations
- Standards for processes, cybersecurity, and test methods

NIST Metrology Director





Dr. Marla L. Dowell

- Director, Communication Technology Laboratory (CTL)
- CTL promotes the development and deployment of advanced communications technologies through leading edge R&D
- Fellow of SPIE, SPIE Women in Optics
- Arthur S. Flemming Award, DOC Silver Medal
- Ph.D. Physics, MIT; B.S. Physics, University of Michigan; M.B.A. University of Colorado Boulder



Interagency Coordination



The impact of the CHIPS R&D program is maximized when integrated with programs across the USG.

We are working closely with DOD, NSF, DOE, and other agencies to realize this integration with guidance and support from the White House and OSTP.

Interagency Coordination

GOALS





Unified messaging on agency roles and responsibilities

Program coordination across agencies

IP and unique capability access across agencies

Fluid partnering with other agencies

Fluid partnering with federally funded institutions



Next Steps



- Coming soon
 - NSTC White Paper in 1st Quarter 2023
 - Additional steps to be shared afterwards

- Learn more
 - Visit CHIPS.gov
 - Read the Implementation Strategy
 - Join our mailing list



Questions and Answers